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**ECE 524   
Instructor: Philip Tracton  
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**Requirements Document   
for  
Implementing Neural Network in Zybo z10 Board using VHDL**

**by:**

**Viranshu Paruparla**

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**1. INTRODUCTION  
  
1.1 Purpose**

Here in are the requirements of an FPGA-based system that is intended to classify Fashion MNIST images. The classification system takes image data over UART and processes it via a neural network and finally displays the individual classified result on a display seven-segment.  
  
**1.2 Scope**

This specification addresses the operation of all of the Fashion MNIST classification system's main parts, such as output display, memory management, neural network processing, and communication interfaces.

**1.3 System Overview**

Fashion MNIST classification system being an embedded solution taking input of 28×28 pixel grayscale images to classify them into ten fashion categories (0-9). After sending the image data from the host computer, the system runs autonomously. A pre-trained neural network model is executed in the system such that the weights are quantized from floating-point to fixed-point representation for efficient hardware implementation.

**2. HIGH-LEVEL REQUIREMENTS**

**REQ-SYS-1: System Initialization:** The system shall properly initialize all subsystems upon power-up or reset.

**REQ-SYS-2: UART Communication:** A full 28x28 pixel image (784 bytes) will be sent to the system via UART at 9600 baud.

**REQ-SYS-3: Neural Network Processing:** The system shall process the received image using a MLP neural network to determine classification.

**REQ-SYS-4: Status Indication:** The system shall provide visual indicators through LEDs showing its current operational state (waiting for image, receiving image, processing, result ready).

**3. COMPONENT REQUIREMENTS**

**3.1 Top-Level Controller (fashion\_mnist\_top)**

**REQ-TOP-1: System Initialization:** The top-level controller shall properly initialize all subsystems upon power-up or reset.

**REQ-TOP-2: Operational State Management:** The top-level controller should manage the operational state of the system which includes:

* Waiting for the data.
* Receiving the data.
* Processing Image data.
* Running Neural Network.
* Displaying results.

**REQ-TOP-3: Status Display:** The top-level controller shall drive LED indicators to show the current system state:

* LED 0: Active when waiting for the image data.
* LED 0,1: Active when receiving or processing image data.
* LED 0,1,2: Active when neural network is processing.
* LED 0,1,2,3: Active when the result is ready.

**REQ-TOP-4: Classification Result Display:** The top-level controller shall display the classification result (0-9) on a seven-segment display when processing is complete.

**3.2 UART Receiver (uart\_receiver)**

**REQ-UART-1: Image Data Reception:** The UART receiver shall be capable of receiving 784 bytes corresponding to the 28×28 pixel image, with pixel values ranging from 0 to 255.

**3.3 Image BRAM Controller (image\_bram\_controller)**

**REQ-BRAM-1: Image Storage:** The image BRAM controller shall store a complete 28×28 pixel image (784 bytes) in memory.

**REQ-BRAM-2: Clock-Crossing:** The image BRAM controller will make provisions for handling clock domain crossing safely between the UART clock domain (125MHz) and the neural network clock domain (36MHz).

**3.4 Neural Network Top (nn\_top)**

**REQ-NN-1: Input Processing:** The input should be grayscale and should be handled as a 28\*28 image containing 784 pixels where pixel values lie between 0 (which means white) and 255 (which means black).

**REQ-NN-2: Classification Output:** The neural network shall classify the input image into the most probable class (for 0-9) by finding the maximum value within the 10 output neurons.

**REQ-NN-3: Processing Control:** The neural network shall report its processing status via measurable busy and result\_valid signals traceable in the top-level controller.

**3.5 MLP Layer (mlp\_layer)**

**REQ-MLP-1: Processing Indication:** MLP layers shall indicate to the neural network controller their processing through monitorable busy and data\_out\_valid signals.

**3.6 Clocking Wizard(clock\_gen)**

**REQ-CLK-1: Clock Generation:** The clock generator must therefore emit 36 MHz generated clock signals from the 125MHz system clock.